Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Cancelled)

2. (Cancelled)

3. (Currently Amended) An offset compensating apparatus ~~as claimed in claim~~ 2 which compensates offset of an inverted signal and a non-inverted signal output from paired output ports of an electronic apparatus, the inverted and the non-inverted signals being in accordance with an input signal to the electronic apparatus, comprising:

a selector for selecting one of the inverted signal and the non-inverted signal from the electronic apparatus;

adjusting means for obtaining a difference value between the inverted signal selected by the selector and a reference signal having no relationship to said inverted signal, and holding said difference value;

comparing means for conducting an error signal indicative of a difference between an non-inverted signal selected by the selector and a signal produced by reflecting said held difference value onto said reference signal; and

calculating means for adding a value corresponding to said error signal to said input signal, wherein

said calculating means [[is]] includes a counter.

4. (Currently Amended) An offset compensating apparatus ~~as claimed in claim~~ 2 which compensates offset of an inverted signal and a non-inverted signal output from paired

output ports of an electronic apparatus, the inverted and the non-inverted signals being in accordance with an input signal to the electronic apparatus, comprising:

a selector for selecting one of the inverted signal and the non-inverted signal from the electronic apparatus;

adjusting means for obtaining a difference value between the inverted signal selected by the selector and a reference signal having no relationship to said inverted signal, and holding said difference value;

comparing means for conducting an error signal indicative of a difference between an non-inverted signal selected by the selector and a signal produced by reflecting said held difference value onto said reference signal; and

calculating means for adding a value corresponding to said error signal to said input signal, wherein

said calculating means [[is]] includes an adding-and-subtracting circuit.

5. (Withdrawn) An offset compensating apparatus as claimed in claim 13, wherein said storage means stores thereinto a half value of the converged value of said error signal.

6. (Currently Amended) An offset compensating apparatus as claimed in claim 3 or 4 ~~any one of claim 2 to claim 4~~, wherein both said ~~holding~~ adjusting means and said comparing means correspond to a comparing circuit comprising:

a differential circuit in which two signals are compared with each other, which are entered into a differential pair formed by a first transistor and a second transistor, the differential circuit having said differential pair and a load circuit of said differential pair;

phase adjusting means which operates said differential circuit as an operational amplifying circuit;

phase inverting means which inverts a phase of an output signal from said differential circuit;

feedback means which feeds back an output signal of said phase inverting means as a substrate biasing voltage of said first transistor in the case that said differential circuit is operated as the operational amplifying circuit by said phase adjusting means, and either same voltages or different voltages are applied to said first transistor and said second transistor of said differential pair respectively; and

holding means for holding said substrate biasing voltage of said first transistor in a predetermined time duration, which is fed back by said feedback means.

7-11. (Cancelled)

12. (Currently Amended) An offset compensating apparatus as claimed in claim 3 or 4 ~~any one of claim 2 to claim 5~~, wherein said electronic apparatus corresponds to a D/A (digital-to-analog) converting circuit.

13. (Withdrawn and Currently Amended) An offset compensating apparatus as claimed in claim [[2]] 3, further comprising

storage means for storing a converged value of said error signal; and

selector for selecting the storage means to add the converged value to the input signal when the value corresponding to said error signal is converged.

14. (Withdrawn) An offset compensating apparatus which compensates offset of an inverted signal and a non-inverted signal output from paired output ports of an electronic apparatus, the inverted and the non-inverted signal being in accordance with an input signal to the electronic apparatus, comprising:

adjusting means for obtaining a difference value between the inverted signal and a reference signal having no relationship to said inverted signal, and holding said difference value;

comparing means for conducting an error signal indicative of a difference between an non-inverted signal and a signal produced by reflecting said held difference value onto said reference signal;

calculating means for adding a value corresponding to said error signal to said input signal;

storage means for storing a converged value of said error signal; and

selector for selecting the storage means to add the converged value to the input signal when the value corresponding to said error signal is converged.

15. (Withdrawn) An offset compensating apparatus as claimed in claim 14, wherein said calculating means is a counter.

16. (Withdrawn) An offset compensating apparatus as claimed in claim 14, wherein said calculating means is an adding-and-subtracting circuit.

17. (Withdrawn) An offset compensating apparatus as claimed in claim 14, wherein said storage means stores a half value of the converged value of said error signal.

18. (Withdrawn) An offset compensating apparatus as claimed in claim 14, wherein both said holding means and said comparing means correspond to a comparing circuit comprising:

a differential circuit in which two signals are compared with each other, which are entered into a differential pair formed by a first transistor and a second transistor, the differential circuit having said differential pair and a load circuit of said differential pair;

phase adjusting means which operates said differential circuit as an operational amplifying circuit;

phase inverting means which inverts a phase of an output signal from said differential circuit;

feedback means which feeds back an output signal of said phase inverting means as a substrate biasing voltage of said first transistor in the case that said differential circuit is operated as the operational amplifying circuit by said phase adjusting means, and either same voltages or different voltages are applied to said first transistor and said second transistor of said differential pair respectively; and

holding means for holding said substrate biasing voltage of said first transistor in a predetermined time duration, which is fed back by said feedback means.

19. (Cancelled)